In the Claims:

The pending claims are as follows.

1. (Previously Presented) A receiver circuit comprising:

an error detection circuit configured to receive a digital signal comprising in-phase (I) and quadrature (Q) components, to combine the digital signal with a complex image correction factor and, dependent upon combining the digital signal with the complex image correction factor, to detect an error in the complex image correction factor; and

an error correction circuit coupled to said error detection circuit and configured to modify said complex image correction factor dependent upon said error;

wherein to combine the digital signal with the complex image correction factor, the error detection circuit is further configured to:

multiply said in-phase component by a value of a first function of a real portion of said complex image correction factor to form a first product;

multiply said in-phase component by a value of a first function of an imaginary portion of said complex image correction factor to form a second product;

multiply said quadrature component by a value of a second function of the real portion of said complex image correction factor to form a third product;

multiply said quadrature component by a value of a second function of the imaginary portion of said complex image correction factor to form a fourth product;

accumulate said first and fourth products; and

accumulate said second and third products.

2. (Original) The receiver circuit as recited in claim 1, wherein said error detection circuit and said error correction circuit are coupled in a feedback loop, wherein said error detection circuit is configured to iteratively detect said error in said complex image correction factor, and wherein said error correction circuit is configured to iteratively correct said error.

3. (Original) The receiver circuit as recited in claim 2, wherein said error detection circuit is configured to iteratively detect said error and said error correction circuit is configured to iteratively correct said error until a threshold time has elapsed.

4. (Previously Presented) The receiver circuit as recited in claim 2, wherein:

said error detection circuit is further configured to square a result of combining said digital signal with said complex image correction factor and to select a complex error component corresponding to said error in said complex image correction factor from said squared result; and

said error correction circuit is further configured to scale said complex error component by a scaling factor and to accumulate said scaled error component into said complex image correction factor.

5. (Canceled)

6. (Original) The receiver circuit as recited in claim 4, wherein said scaling factor is programmable.

7. (Original) The receiver circuit as recited in claim 6, wherein said scaling factor is programmed with different values during successive iterations.

8. (Original) The receiver circuit as recited in claim 4, wherein said digital signal is dependent upon a calibration tone, and wherein selecting an error component from said squared result comprises providing a notch filter tuned to select said error component.

9. (Original) The receiver circuit as recited in claim 4, wherein said digital signal is dependent upon a radio frequency signal input, wherein selecting an error component from said squared result comprises detecting whether a radio frequency signal is present, and wherein accumulating said scaled error component into said complex image correction factor occurs dependent on said detecting.

10. (Previously Presented) A method comprising:

receiving a digital signal comprising in-phase (I) and quadrature (Q) components;

combining said digital signal with a complex error correction factor;

detecting an error in said complex image correction factor in response to said combining; and

modifying said complex image correction factor dependent upon said error;

wherein combining said digital signal with said complex image correction factor further comprises:

multiplying said in-phase component by a value of a first function of a real portion of said complex image correction factor to form a first product;

multiplying said in-phase component by a value of a first function of a imaginary portion of said complex image correction factor to form a second product;

multiplying said quadrature component by a value of a second function of the real portion of said complex image correction factor to form a third product;

multiplying said quadrature component by a value of a second function of the imaginary portion of said complex image correction factor to form a fourth product;

accumulating said first and fourth products; and

accumulating said second and third products.

11. (Original) The method as recited in claim 10, wherein said combining further comprises iteratively combining said digital signal with said modified complex image correction factor, wherein said detecting an error further comprises iteratively detecting an error in said modified complex image correction factor, and wherein said modifying said complex image correction factor further comprises iteratively modifying said complex image correction factor dependent upon said error.

12. (Original) The method as recited in claim 11, wherein said iterative combining, iterative detecting, and iterative modifying continue until a threshold time has elapsed.

13. (Original) The method as recited in claim 10, wherein detecting an error further comprises squaring a result of said combining and selecting a complex error component corresponding to said error in said complex image correction factor from said squared result, and wherein modifying said complex image correction factor further comprises scaling said complex error component by a scaling factor and accumulating said scaled error component into said complex image correction factor.

14. (Original) The method as recited in claim 13, wherein said scaling factor is programmable.

15. (Original) The method as recited in claim 14, wherein said scaling factor is programmed with different values during successive iterations.

16. (Canceled)

17. (Original) The method as recited in claim 13, wherein said digital signal is dependent upon a calibration tone, and wherein selecting an error component from said squared result comprises providing a notch filter tuned to select said error component.

18. (Original) The method as recited in claim 13, wherein said digital signal is dependent upon a radio frequency signal input, wherein selecting an error component from said squared result comprises detecting whether a radio frequency signal is present, and wherein accumulating said scaled error component into said complex image correction factor occurs dependent on said detecting.

19. (Previously Presented) A computer-accessible medium comprising program instructions, wherein the program instructions are executable by a processor to:

receive a digital signal comprising in-phase (I) and quadrature (Q) components;

combine said digital signal with a complex image correction factor;

detect an error in said complex image correction factor dependent upon combining said digital signal with said complex image correction factor; and

modify said complex image correction factor dependent upon said error;

wherein to combine said digital signal with said complex image correction factor, the program instructions are further executable to:

multiply said in-phase component by a value of a first function of a real portion of said complex image correction factor to form a first product;

multiply said in-phase component by a value of a first function of a imaginary portion of said complex image correction factor to form a second product;

multiply said quadrature component by a value of a second function of the real portion of said complex image correction factor to form a third product;

multiply said quadrature component by a value of a second function of the imaginary portion of said complex image correction factor to form a fourth product;

accumulate said first and fourth products; and

accumulate said second and third products.

20. (Original) The computer-accessible medium as recited in claim 19, wherein said processor is a digital signal processor (DSP).